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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/686,866	10/16/2003	Chung Long Chang	24061. / TSMC2002-1305	7401
42717	7590	08/07/2006	EXAMINER	
HAYNES AND BOONE, LLP 901 MAIN STREET, SUITE 3100 DALLAS, TX 75202			CRANE, SARA W	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

NC ✓

**Advisory Action  
Before the Filing of an Appeal Brief**

Application No. 10/686,866		Applicant(s) CHANG ET AL.	
Examiner Sara W. Crane		Art Unit 2811	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 13 July 2006 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 5 mos months from the mailing date of the final rejection.  
b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**NOTICE OF APPEAL**

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

**AMENDMENTS**

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
(a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);  
(b) ☐ They raise the issue of new matter (see NOTE below);  
(c) ☒ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
(d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).


4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
The status of the claim(s) is (or will be) as follows:  
Claim(s) allowed: \_\_\_\_\_.  
Claim(s) objected to: \_\_\_\_\_.  
Claim(s) rejected: \_\_\_\_\_.  
Claim(s) withdrawn from consideration: \_\_\_\_\_.

**AFFIDAVIT OR OTHER EVIDENCE**

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

**REQUEST FOR RECONSIDERATION/OTHER**

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). \_\_\_\_\_.  
13. ☐ Other: \_\_\_\_\_.

  
Sara W. Crane  
Primary Examiner  
Art Unit: 2811

Continuation of 3. NOTE: A number of claims that previously depended from claim 4 now depend from claim 7. Claim 7 includes, for example, the limitation "wherein the second electrode is within the perimeter of the first electrode . . . ." The combination of this feature with each of the limitations of claims 2, 3, 5, 6, 9, and 10 has not been previously considered..

Continuation of 11. does NOT place the application in condition for allowance because: Applicant argues that one of the goals of the Morimoto teachings, that of suppressing the voltage dependence of a capacitance value more than for conventional MIM capacitors, could not be achieved if the second electrode is within the perimeter of the first electrode, as recited in the last line of claim 7. Examiner can see no reason why this would be so. The basic Morimoto teaching is that voltage dependence can be reduced by connecting two MIM capacitors in parallel (column 3, lines 28-31). This has nothing whatever to do with whether the perimeter of one electrode is within the perimeter of another electrode, because the parallel connection between the two capacitors is independent of the electrode shape. However, even if one desires a relative area ratio of 2 to 15, say, as desired by Morimoto for one of the embodiments, this can be obtained at the same time as the perimeter relationship. This is not a "teaching away" type of situation, this is a simply situation where one of ordinary skill would obtain two goals simultaneously, as in the usual patentability analysis where obviousness is the issue.

Applicant also argues that the motivation for combining the teachings, for example, the desire to allow room for multiple contacts to a lower capacitor layer, is derived from Applicant's specification. Examiner did not find any such teaching in Applicant's specification. The area for multiple contacts is apparent to one of ordinary skill on looking at Hieda figure 1, for example, where the desire to decrease contact resistance is well-known in the art, because higher contact resistance is associated with greater heating when current flows.

The layers of claim 19 are the same as discussed previously with respect to prior claims, as for example claim 4. As noted in the final Office action, a transistor would have been obvious because the capacitor is taught to be used in an active integrated circuit. Any such transistor would have to have a contact feature of some sort, in order to be a useful transistor, and such a contact feature would have to connect somehow to one end or the other of the Morimoto capacitor, to implement a circuit having both a transistor and a capacitor. The top contact of the Morimoto capacitor is directly connected to layer 15-3, identified to the second interconnect.